STIC Search Report
EIC 2100

USPTO

STIC Database Tracking Number: 126478

TO: Cynthia Britt **Location: 4A12** **Art Unit : 2133** **Tuesday, July 06, 2004** **Case Serial Number: 10/073830**	**From: Geoffrey St. Leger** **Location: EIC 2100** **PK2-4B30** **Phone: 308-7800** **geoffrey.stleger@uspto.gov**

Search Notes

Dear Examiner Britt,

Attached please find the results of your search request for application 10/073830. I searched Dialog's foreign patent files, technical databases, product announcement files and general files; along with the Internet.

Please let me know if you have any questions.

Regards,

Geoffrey St. Leger
4B30/308-7800

sira
Search and Information Resources Administration

```
File   8:Ei Compendex(R) 1970-2004/Jun W4
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
File 202:Info. Sci. & Tech. Abs. 1966-2004/May 14
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         (c) 2004 Institution of Electrical Engineers
File 233:Internet & Personal Comp. Abs. 1981-2003/Sep
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File  94:JICST-EPlus 1985-2004/Jun W2
         (c)2004 Japan Science and Tech Corp(JST)
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         (c) 2004 INIST/CNRS
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         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Jun W4
         (c) 2004 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Jun
         (c) 2004 The HW Wilson Co.
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
File 266:FEDRIP 2004/Apr
         Comp & dist by NTIS, Intl Copyright All Rights Res
File  95:TEME-Technology & Management 1989-2004/Jun W1
         (c) 2004 FIZ TECHNIK
File 438:Library Lit. & Info. Science 1984-2004/Jun
         (c) 2004 The HW Wilson Co
File 104:AeroBase 1999-2004/May
         (c) 2004 Contains copyrighted material
File  62:SPIN(R) 1975-2004/May W2
         (c) 2004 American Institute of Physics
File 239:Mathsci 1940-2004/Aug
         (c) 2004 American Mathematical Society

Set     Items   Description
S1       3417   BOUNDARY()SCAN OR (IEEE OR ENGINEER???)(2W)1149
S2     577326   GRAPHIC? OR GUI? ?
S3      18982   S2(10N)(FAULT? ? OR FAIL??? OR VIOLAT? OR ERROR? ? OR DEFE-
             CT? OR PROBLEM? OR FLAW? ? OR IRREGULAR? OR INVALID? OR ("NOT"
              OR T)(1W)(VALID OR ACCURAT?) OR INACCURAT? OR ABNORMAL?)
S4         12   S1 AND S3
S5          7   RD (unique items)
```

5/5/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06602019 E.I. No: EIP03457716280
Title: A Comprehensive Approach to Assessing and Analyzing 1149.1 Test Logic
Author: Melocco, Kevin; Arora, Hina; Setlak, Paul; Kunselman, Gary; Mardhani, Shazia
Corporate Source: Cadence Design Systems Test Design Automation, Endicott, NY 13760, United States
Conference Title: Proceedings International Test Conference 2003
Conference Location: Charlotte, NC, United States Conference Date: 20030930-20031002
Sponsor: IEEE Computer Society Test Technology Technical Council; IEEE Philadelphia Section
E.I. Conference No.: 61696
Source: IEEE International Test Conference (TC) 2003. p 358-367 (IEEE cat n 03CH37494)
Publication Year: 2003
CODEN: PITCFN ISSN: 1089-3539
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 0311W3
Abstract: In this paper we introduce a tool which is capable of verifying an 1149.1 test logic implementation and its compliance to the **IEEE 1149** .1 Standard left bracket 1 right bracket left bracket 2 right bracket while providing a precise list of **errors** as well as good debug and diagnostic information using **graphical** analysis. The paper provides a review of the methods used to perform the logic verification. We introduce an efficient technique for verifying the correspondence of chip I/O with the **boundary scan** register and for verifying large scan registers. The tool is independent of how the test logic is instantiated. The tool requires only the design netlist, cell library definition, and its BSDL left bracket 2 right bracket identifying what 1149.1 test logic has been implemented. Results on current large ASIC designs is included left bracket 10 right bracket . 12 Refs.
Descriptors: *Program debugging; Microprocessor chips; Graph theory; Error analysis; Computer simulation
Identifiers: Logic verification
Classification Codes:
723.1 (Computer Programming); 714.2 (Semiconductor Devices & Integrated Circuits); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory); 921.6 (Numerical Methods); 723.5 (Computer Applications)
723 (Computer Software, Data Handling & Applications); 714 (Electronic Components & Tubes); 921 (Applied Mathematics)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATION ENGINEERING); 92 (ENGINEERING MATHEMATICS)

5/5/3 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03790386 E.I. No: EIP94011194369
Title: Multiple fault diagnosis in printed circuit boards
Author: Barnfield, S.J.; Moore, W.R.
Corporate Source: Univ of Oxford, Oxford, UK
Conference Title: Proceedings of the 24th IEEE International Test Conference
Conference Location: Baltimore, MD, USA Conference Date: 19931017-19931021
E.I. Conference No.: 19689
Source: Proceedings of the International Test Conference 1993. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA,(IEEE cat n 93CH3356-3). p 662-671
Publication Year: 1993
CODEN: 001300 ISBN: 0-7803-1429-8

Language: English
Document Type: CA; (Conference Article) Treatment: G; (General Review); T; (Theoretical)
Journal Announcement: 9403W2
Abstract: This paper addresses the problems of diagnosing multiple faults occurring in the non- **boundary - scan** parts of a printed circuit board. The paper details a diagnostic algorithm based upon combining the fault signatures of single faults in order to produce a pattern which best matches the signature of a multiple **fault** . In addition, a **graphical** routine is presented which allows the tester to analyze a given set of test vectors. This analysis provides an implicit fault-simulation process for stuck-at and bridging faults. Furthermore, the process informs the tester of any faults which mask other previously detectable faults within the given test set. (Author abstract) 17 Refs.
Descriptors: *Printed circuit testing; Printed circuit design; Electric fault currents; Electric fault location; Mathematical models; Algorithms
Identifiers: Multiple fault diagnosis; Fault signatures; Test vectors
Classification Codes:
713.5 (Other Electronic Circuits); 701.1 (Electricity: Basic Concepts & Phenomena); 921.6 (Numerical Methods); 723.1 (Computer Programming)
713 (Electronic Circuits); 701 (Electricity & Magnetism); 921 (Applied Mathematics); 723 (Computer Software)
71 (ELECTRONICS & COMMUNICATIONS); 70 (ELECTRICAL ENGINEERING); 92 (ENGINEERING MATHEMATICS); 72 (COMPUTERS & DATA PROCESSING)

5/5/5 **(Item 1 from file: 2)**
DIALOG(R)File 2:INSPEC

7712478 INSPEC Abstract Number: B2003-09-2570D-024, C2003-09-7410D-092
Title: New graphical I/sub DDQ/ signatures reduce defect level and yield loss
Author(s): Rao, L.; Bushnell, M.L.; Agrawal, V.D.
Author Affiliation: Dept. of Electr. & Comput. Eng., Rutgers Univ., Piscataway, NJ, USA
Conference Title: Proceedings 16th International Conference on VLSI Design concurrently with the 2nd International Conference on Embedded Systems Design p.353-60
Publisher: IEEE Comput. Soc, Los Alamitos, CA, USA
Publication Date: 2003 Country of Publication: USA xxvi+595 pp.
ISBN: 0 7695 1868 0 Material Identity Number: XX-2002-03966
U.S. Copyright Clearance Center Code: 1063-9667/03/$17.00
Conference Title: Proceedings 16th International Conference on VLSI Design. Concurrently with the 2nd International Conference on Embedded Systems Design
Conference Sponsor: VLSI Soc. India (VSI) Minstr. Commun. & Inf. Technol., Govern. India; IEEE Circuits & Syst. Soc.; ACM SIGDA; NASSCOM
Conference Date: 4-8 Jan. 2003 Conference Location: New Delhi, India
Medium: Also available on CD-ROM in PDF format
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: The measured I/sub DDQ/ current as a function of vectors is defined here as the I/sub DDQ/ signature of a chip. We examined the I/sub DDQ/ signatures of a large number of SEMATECH chips that have been classified as good or bad by a combined decision from functional, delay and scan tests. We find that a single I/sub DDQ/ threshold, whether absolute or differential, cannot separate good/bad chips with any desirable accuracy, because the good chip signature can be any one of several well-defined graphs. In general, the signature of a good chip is found to contain, discrete levels (or bands) of varying widths and separations. A faulty chip almost always displays noise and glitches in the band structure. Based on observations, we develop a set of five **graphical** criteria, which provide lower **defect** level and yield loss compared to other non-I/sub DDQ/ test methods. The reason is that the graphical procedure customizes the decision for the chip-under-test, and may substantially reduce the usage of other conventional tests. (12 Refs)
Subfile: B C

Descriptors: automatic testing; **boundary scan** testing; CMOS integrated circuits; delays; integrated circuit testing; integrated circuit yield

Identifiers: graphical I/sub DDQ/ signatures; defect level; yield loss; SEMATECH chips; functional tests; delay tests; scan tests; chip signature; discrete levels; glitches; chip-under-test

Class Codes: B2570D (CMOS integrated circuits); B7210A (Automatic test systems); B2570A (Semiconductor integrated circuit design, layout, modelling and testing); C7410D (Electronic engineering computing)

5/5/6 (Item 2 from file: 2)

DIALOG(R)File 2:INSPEC

04249697 INSPEC Abstract Number: B9211-0170J-048

Title: Improving MCM assembly yields through approaches for known-good ICs

Author(s): Wagner, R.J.; Hagge, J.K.

Author Affiliation: Rockwell Int. Corp., Cedar Rapids, IA, USA

Conference Title: Proceedings of the Technical Conference. 1991 International Electronic Packaging Conference p.882-97 vol.2

Publisher: Int. Electron. Packaging Soc, Wheaton, IL, USA

Publication Date: 1991 Country of Publication: USA 2 vol. 1134 pp.

Conference Date: 15-18 Sept. 1991 Conference Location: San Diego, CA, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Applications (A); Bibliography (B); Practical (P)

Abstract: This paper discusses the problems, issues, and advances needed to bring 'Known-Good ICs' to the MCM assembly process. IC vendor business issues, IC user procurement concerns and the issue of industry standards are presented. IC yield and its effect on MCM production rework and **defect** level are shown **graphically** . Assembly yields of MCM packaging technology must approach the yields obtainable in alternate packaging technology choices to be cost and benefit competitive. Resolving the technical issues of producing known-good ICs for MCMs involves approaches performed either prior to, or after, dicing of the IC wafer into individual chips. IC design-for-testability approaches presented include built-in-self-test and **boundary - scan** . Wafer level reliability and other process monitors are explored. Metallurgical techniques to improve the test access for screening unpackaged dice including; TAB, micro chip carriers, flying lead approaches and chip-on-tape are discussed. (64 Refs)

Subfile: B

Descriptors: assembling; circuit reliability; integrated circuit technology; integrated circuit testing; modules; packaging

Identifiers: known-good integrated circuits; IC design-for-testability; pressure contact method; anisotropic conductive film; membrane probe method ; wafer level reliability; MCM assembly yields; MCM assembly process; IC vendor business issues; industry standards; MCM production rework; MCM packaging technology; IC wafer; built-in-self-test; **boundary - scan** ; TAB; micro chip carriers; flying lead approaches; chip-on-tape

Class Codes: B0170J (Product packaging); B2570 (Semiconductor integrated circuits); B0170E (Production facilities and engineering); B2220J (Hybrid integrated circuits)

5/5/7 (Item 1 from file: 95)

DIALOG(R)File 95:TEME-Technology & Management

00890681 E95050229211

Reparieren nach dem Boundary - Scan **-Test. Computer Aided Repair vermeidet Reparaturfehler**

Halaczek, T; Sandner, B

Philips Semiconductors, Nuernberg, D; IPC Klaus Mauderer, Nuernberg, D

Elektronik, Muenchen, v44, n9, pp104-107, 1995

Document type: journal article Language: German

Record type: Abstract

ISSN: 0013-5658

ABSTRACT:
Der **Boundary - Scan** -Test (BST) hat schon revolutionaere Auswirkungen in manchen Anwendungsbereichen verursacht. Damit BST aber billig realisiert werden kann, muessen die Vorteile einer kurzen Testentwicklungsphase und einer kurzen Testzeit um die Pluspunkte einer billigen Test-Hardware und eines kostenguenstigen Reparaturablaufes ergaenzt werden. Die Reparatur selbt darf, um wirtschaftlich zu bleiben, nur sehr wenig Zeit in Anspruch nehmen. Entsprechend bietet sich eine Softwareloesung aus der Gruppe der Computer-Aided-Repair-Systeme an. Da es zur Zeit keine einfachen, BST-faehigen Reparaturstationen gibt, wird im folgenden Beitrag ein aeusserst benutzerfreundliches Reparatursystem im Sinne des Computer-Aided-Repair vorgestellt. Das Hauptinteresse bei der Realisierung der Reparaturstation galt vor allem der grafischen Fehlerlokalisation auf dem Bildschirm.

TRANSLATED BY GOOGLE

5/5/7 (Item 1 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00890681 E95050229211
Repair after the Boundary - Scan test. Computer Aided Repair avoids repair errors
Halaczek, T; Sandner, B
Philips Semiconductors, Nuernberg, D; IPC Klaus Mauderer, Nuernberg, D
Elektronik, Muenchen, v44, n9, pp104-107, 1995
Document type: journal article Language: German
Record type: Abstract
ISSN: 0013-5658

ABSTRACT:

The Boundary - Scan test (BST) caused already revolutionary effects in some ranges of application. So that BST can be realized however cheaply, the advantages of a short test development phase must and a short testing time around the pluses of a cheap test hardware and a economical expiration of repair to be supplemented. The repair selbt may, in order to remain economical, to take only very little time up. Accordingly a software solution from the group of the computer Aided Repair systems offers itself. There there at present no simple, BST able repair act ions is, in the following contribution an extremely user friendly repair system in the sense of the computer Aided Repair is introduced. **The principal interest with the realization of the repair station applied above all for the graphic error localization on the screen.**

```
File   8:Ei Compendex(R) 1970-2004/Jun W4
         (c) 2004 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/May
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Jul W1
         (c) 2004 BLDSC all rts. reserv.
File   2:INSPEC 1969-2004/Jun W4
         (c) 2004 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2004/Jun W2
         (c)2004 Japan Science and Tech Corp(JST)
File   6:NTIS 1964-2004/Jun W4
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2004/Jun W4
         (c) 2004 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Jun W4
         (c) 2004 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Jun
         (c) 2004 The HW Wilson Co.
File 266:FEDRIP 2004/Apr
         Comp & dist by NTIS, Intl Copyright All Rights Res
File  95:TEME-Technology & Management 1989-2004/Jun W1
         (c) 2004 FIZ TECHNIK
File 104:AeroBase 1999-2004/May
         (c) 2004 Contains copyrighted material
File  62:SPIN(R) 1975-2004/May W2
         (c) 2004 American Institute of Physics
File 239:Mathsci 1940-2004/Aug
         (c) 2004 American Mathematical Society

Set     Items   Description
S1       3404   BOUNDARY()SCAN OR (IEEE OR ENGINEER???)(2W)1149
S2        307   AU=(COGSWELL, M? OR MARDHANI, S? OR MELOCCO, K? OR ARORA, -
                  H? OR COGSWELL M? OR MARDHANI S? OR MELOCCO K? OR ARORA H?)
S3          6   S1 AND S2
S4          3   RD (unique items)
```

4/5/1 **(Item 1 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)

06602019 E.I. No: EIP03457716280
Title: A Comprehensive Approach to Assessing and Analyzing 1149.1 Test Logic
Author: **Melocco, Kevin** ; **Arora, Hina** ; Setlak, Paul; Kunselman, Gary; **Mardhani, Shazia**
Corporate Source: Cadence Design Systems Test Design Automation, Endicott, NY 13760, United States
Conference Title: Proceedings International Test Conference 2003
Conference Location: Charlotte, NC, United States Conference Date: 20030930-20031002
Sponsor: IEEE Computer Society Test Technology Technical Council; IEEE Philadelphia Section
E.I. Conference No.: 61696
Source: IEEE International Test Conference (TC) 2003. p 358-367 (IEEE cat n 03CH37494)
Publication Year: 2003
CODEN: PITCFN ISSN: 1089-3539
Language: English
Document Type: CA; (Conference Article) Treatment: T; (Theoretical)
Journal Announcement: 0311W3
Abstract: In this paper we introduce a tool which is capable of verifying an 1149.1 test logic implementation and its compliance to the **IEEE 1149** .1 Standard left bracket 1 right bracket left bracket 2 right bracket while providing a precise list of errors as well as good debug and diagnostic information using graphical analysis. The paper provides a review of the methods used to perform the logic verification. We introduce an efficient technique for verifying the correspondence of chip I/O with the **boundary scan** register and for verifying large scan registers. The tool is independent of how the test logic is instantiated. The tool requires only the design netlist, cell library definition, and its BSDL left bracket 2 right bracket identifying what 1149.1 test logic has been implemented. Results on current large ASIC designs is included left bracket 10 right bracket . 12 Refs.
Descriptors: *Program debugging; Microprocessor chips; Graph theory; Error analysis; Computer simulation
Identifiers: Logic verification
Classification Codes:
723.1 (Computer Programming); 714.2 (Semiconductor Devices & Integrated Circuits); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory); 921.6 (Numerical Methods); 723.5 (Computer Applications)
723 (Computer Sóftware, Data Handling & Applications); 714 (Electronic Components & Tubes); 921 (Applied Mathematics)
72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATION ENGINEERING); 92 (ENGINEERING MATHEMATICS)

4/5/2 **(Item 2 from file: 8)**
DIALOG(R)File 8:Ei Compendex(R)

06247334 E.I. No: EIP02517276973
Title: A structured graphical tool for analyzing boundary scan **violations**
Author: **Cogswell, Michael** ; **Mardhani, Shazia** ; **Melocco, Kevin** ; **Arora, Hina**
Corporate Source: Test Design Automation IBM Corp., Endicott, NY 13760, United States
Conference Title: Proceedings International Test Conference
Conference Location: Baltimore, MD, United States Conference Date: 20021007-20021010
Sponsor: IEEE
E.I. Conference No.: 60343
Source: IEEE International Test Conference (TC) 2002. p 755-762 (IEEE cat n 02ch37382)

Publication Year: 2002
CODEN: PITCFN ISSN: 1089-3539
Language: English
Document Type: CA; (Conference Article) Treatment: A; (Applications); T ; (Theoretical)
Journal Announcement: 0301W1
Abstract: The **Boundary Scan** Test methodology is becoming an increasingly important approach for testing chips, modules and boards. Commercial **Boundary Scan** verification tools are now available which provide a system of checks not only for **IEEE 1149** .1 but other methodologies such as IBM **Boundary Scan** . A key factor in the effectiveness of **Boundary Scan** Verification systems is found in the accuracy and flexibility of companion analysis tools used to correlate the violated **Boundary Scan** rule with the subject logic structure causing the violation. This paper presents the design and deployment of a graphical system for pinpointing sources of **Boundary Scan** rules violations. The paper begins with a cursory review of **Boundary Scan** methodologies including **IEEE 1149** .1 and IBM **Boundary Scan** . This is followed by a brief presentation of the **Boundary Scan** verification process used in IBM's TestBench tool. The body of the paper is focused on **Boundary Scan** verification rules and the associated message analysis. The paper concludes with future plans under consideration to improve both the reach and usability of graphical message analysis for **Boundary Scan** verification. 6 Refs.
Descriptors: *Design for testability; Graph theory; Electric codes; Finite automata; Computer hardware description languages; Application specific integrated circuits; Multichip modules; Computer simulation
Identifiers: **Boundary Scan** Test; **Boundary Scan** Verification System; Test Access Port; Test Data In; Test Data Out
Classification Codes:
723.1.1 (Computer Programming Languages)
721.2 (Logic Elements); 921.4 (Combinatorial Mathematics, Includes Graph Theory, Set Theory); 902.2 (Codes & Standards); 721.1 (Computer Theory (Includes Formal Logic, Automata Theory, Switching Theory & Programming Theory)); 723.1 (Computer Programming)
721 (Computer Circuits & Logic Elements); 921 (Applied Mathematics); 902 (Engineering Graphics; Engineering Standards; Patents); 723 (Computer Software, Data Handling & Applications)
72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS); 90 (ENGINEERING, GENERAL)

4/5/3 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

04353600 INSIDE CONFERENCE ITEM ID: CN045603611
A Structured Graphical Tool for Analyzing Boundary - Scan **Violations**
Mardhani, S. ; Cogswell, M. ; Melocco, K. ; Arora, H.
CONFERENCE: International test conference
INTERNATIONAL TEST CONFERENCE, 2002 P: 755-762
IEEE, 2002
ISSN: 1089-3539 ISBN: 0780375424
LANGUAGE: English DOCUMENT TYPE: Conference Papers
CONFERENCE SPONSOR: IEEE
CONFERENCE LOCATION: Baltimore, MD 2002; Oct (200210) (200210)

BRITISH LIBRARY ITEM LOCATION: 4550.438000
NOTE:
Also known as ITC. IEEE cat no 02CH37382
DESCRIPTORS: test; IEEE; ITC

File 347:JAPIO Nov 1976-2004/Feb(Updated 040607)
(c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200442
(c) 2004 Thomson Derwent

Set	Items	Description
S1	840	BOUNDARY()SCAN OR (IEEE OR ENGINEER???)(2W)1149
S2	4	AU=(COGSWELL, M? OR MARDHANI, S? OR MELOCCO, K? OR ARORA, - H? OR COGSWELL M? OR MARDHANI S? OR MELOCCO K? OR ARORA H?)
S3	0	S1 AND S2

File 348:EUROPEAN PATENTS 1978-2004/Jun W03
(c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040701,UT=20040624
(c) 2004 WIPO/Univentio

Set	Items	Description
S1	804	BOUNDARY()SCAN OR (IEEE OR ENGINEER???)(2W)1149
S2	0	AU=(COGSWELL, M? OR MARDHANI, S? OR MELOCCO, K? OR ARORA, - H? OR COGSWELL M? OR MARDHANI S? OR MELOCCO K? OR ARORA H?)
S3	0	S1 AND S2

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File 275:Gale Group Computer DB(TM) 1983-2004/Jul 05
         (c) 2004 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2004/Jul 02
         (c) 2004 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2004/Jul 05
         (c) 2004 The Gale Group
File  16:Gale Group PROMT(R) 1990-2004/Jul 05
         (c) 2004 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 148:Gale Group Trade & Industry DB 1976-2004/Jul 02
         (c)2004 The Gale Group
File 624:McGraw-Hill Publications 1985-2004/Jun 24
         (c) 2004 McGraw-Hill Co. Inc
File  15:ABI/Inform(R) 1971-2004/Jun 27
         (c) 2004 ProQuest Info&Learning
File 647:CMP  Computer Fulltext 1988-2004/Jun W4
         (c) 2004 CMP Media, LLC
File 674:Computer News Fulltext 1989-2004/Jun W2
         (c) 2004 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2004/Jul 05
         (c) 2004 The Dialog Corp.
File 369:New Scientist 1994-2004/Jun W4
         (c) 2004 Reed Business Information Ltd.
File 810:Business Wire 1986-1999/Feb 28
         (c) 1999 Business Wire
File 610:Business Wire 1999-2004/Jul 05
         (c) 2004 Business Wire.
File 613:PR Newswire 1999-2004/Jul 05
         (c) 2004 PR Newswire Association Inc
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc

Set     Items   Description
S1       4886   BOUNDARY()SCAN OR (IEEE OR ENGINEER???)(2W)1149
S2    1454837   GRAPHIC? OR GUI? ?
S3      29178   S2(10N)(FAULT? ? OR FAIL??? OR VIOLAT? OR ERROR? ? OR DEFE-
             CT? OR PROBLEM? OR FLAW? ? OR IRREGULAR? OR INVALID? OR ("NOT"
              OR T)(1W)(VALID OR ACCURAT?) OR INACCURAT? OR ABNORMAL?)
S4         42   S1(100N)S3
S5         29   RD (unique items)
```

5/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01673924 SUPPLIER NUMBER: 15091825 (USE FORMAT 7 OR 9 FOR FULL TEXT)
DFT tool automates partial- and boundary-scan vector generation. (AT&T Design Automation introduces ATTDFT for Circuit Design design-for-test tool) (Product Announcement)
Donlin, Mike
Computer Design, v33, n3, p120(1)
March, 1994
DOCUMENT TYPE: Product Announcement ISSN: 0010-4566 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 663 LINE COUNT: 00054

... a deselection or destructive approach to flip-flop selection require 80 percent to 90 percent of flip-flops be scanned for the same coverage.

* Automatic **boundary** scan

The BCAD1 tool in the ATTDFT for Circuit Design system contains a graphical **Boundary Scan** Description Editor for creating and editing **Boundary Scan** Description Language (BSDL) files at the functional level. The tool also generates test vectors to verify that a design conforms to the **IEEE 1149** .1 **boundary - scan** standard. In addition to the conformance test, these vectors ensure the implementation of the **boundary scan** matches the BSDL description and automatically provides high fault coverage for the device's **boundary - scan** logic. Extensive semantic checks included within the editor ensure an error free file. Conformance test generation is accessed via the same graphical user interface as the Boundary.

According to AT&T, the tool's automated functions are aimed at design engineers, who may want to adopt **boundary - scan** techniques, but are reluctant to learn complicated manual tools. "Other approaches require the use of time-consuming and error-prone manual methods to create the...

...introduced during the synthesis process," says Hector Ruiz-Puyana, product manager for IC test tools at AT&T. "By automating the process, we can introduce **boundary scan** into a device faster and more accurate and with 100 percent compliance to the standard. During the next 18 months, we plan to incorporate other...

5/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01669504 SUPPLIER NUMBER: 15024869 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Testing dilemmas and corporate alliances fuel boundary scan's acceptance. (includes related article on Institute of Electrical and Electronics Engineers 1149.1 boundary scan standard)
Donlin, Mike
Computer Design, v33, n1, p65(5)
Jan, 1994
ISSN: 0010-4566 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 3774 LINE COUNT: 00299

... tool vendors have taken a wait-and-see attitude before committing resources to 1149.1-support software. Synopsys was one of the first to offer **boundary - scan** development tools with its Test Compiler Plus **boundary - scan** synthesis product. With Test Compiler Plus, you can optimize a device for area, performance and testability by specifying fault coverage as an additional constraint. The tool then automatically selects the optimal scan architecture for obtaining the desired target **fault** coverage without breaking area or performance constraints.

Mentor **Graphics** has also introduced some **boundary - scan** -related products, developed in partnership with Teradyne. Its Virtual Test Manager, TOP, is built around Teradyne's Victory software and Mentor's Design Architect suite...

5/3,K/3 (Item 3 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01610381 SUPPLIER NUMBER: 14017651 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Tester takes aim at multichip modules. (HP's HP 82000 MCM multichip module testing system) (Product Announcement)
Novellino, John
Electronic Design, v41, n10, p102(2)
May 13, 1993
DOCUMENT TYPE: Product Announcement ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 958 LINE COUNT: 00079

... the HP 82000 MCM's power is software capability typically found only in board test systems. The software facilities MCM testing in three primary ways:

* **Boundary - scan** software called InterconnectPlus offers automatic generation of **IEEE - 1149** .1 component, test-access port, and integrity tests.

* Concurrent test engineering (CTE) tools link the HP 82000 MCM to CAE products such as those from Mentor **Graphics** .

* **Fault** -diagnostic tools, including backtracing software and **fault** dictionaries, permit fast and accurate isolation of failures with or without probe access.

The system's **boundary - scan** software supplies high fault coverage for manufacturing defects on MCMs with limited node access. It performs interconnect tests that find shorts (and most opens) between **boundary - scan** devices. The package also offers an unpowered shorts test and verifies that the **boundary - scan** chain is intact. Where physical access is available, the software will detect opens and test non- **boundary - scan** ICs.

Using the CTE tools, designers can anticipate the tester's capability and avoid creating an untestable device. The software simulates the characteristics of the...

5/3,K/4 (Item 4 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2004 The Gale Group. All rts. reserv.

01556732 SUPPLIER NUMBER: 14414427 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Testing the waters at sea-front show. (Test 92) (Products: Test 92)
Gregg, Paul
Electronics Weekly, n1614, p27(1)
Oct 21, 1992
ISSN: 0013-5224 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 679 LINE COUNT: 00056

ABSTRACT: Test 92 held at the Metropole Hotel in Brighton, England from Oct 20 to 21, 1992 featured the latest products in semiconductor **boundary scan** testing, a manufacturing **defects** analyser as well as **graphic** programming softwares. Test and measurement products were also presented in the exhibition. A fixturing product, designed as a universal replacement for the current generation vacuuum...

5/3,K/5 (Item 1 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)
(c) 2004 The Gale Group. All rts. reserv.

03283997 Supplier Number: 92809151 (USE FORMAT 7 FOR FULLTEXT)
Mentor Graphics Announces Design-for-Test Support for Artisan Components' Flex-Repair Memories.
Business Wire, p0199
Sept 17, 2002

Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 704

... and EDA solutions, eSilicon Corporation. "Because these customers demand best-in-class technology, we're thrilled that we can now offer Artisan memories with Mentor **Graphics** MBISTArchitect to identify and repair manufacturing **defects** with premium, accurate test results without negatively impacting crucial design time."
About Mentor Graphics Design-for-Test Tools
MBISTArchitect is part of the most comprehensive...

...in the market. For today's complex System-on-Chip (SoC) and deep-submicron designs, Mentor Graphics offers DFT solutions for memory BIST, logic BIST, **boundary scan** , automatic test pattern generation (ATPG) and embedded deterministic test (EDT(TM)). Mentor Graphics DFT centers of Excellence are located worldwide and employ the industry's...

5/3,K/6 (Item 2 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

02902205 Supplier Number: 75301606 (USE FORMAT 7 FOR FULLTEXT)
Fluence Technology Cuts Analog Test Time With On-Chip Analog-to-Digital Converter BIST.
Business Wire, p0158
June 6, 2001
Language: English Record Type: Fulltext
Document Type: Newswire; Trade
Word Count: 574

... linearity, offset, gain, transfer function and missing codes. In addition to these histograms, the ADCBIST tests all of the output codes, which can then be **graphically** displayed to clearly identify the types of **defects** and distortion contained in the converter-under-test.
Fluence's ADCBIST is digitally invoked and controlled, making it ideal for ADC production testing, characterization, verification and diagnostics using a standard digital ATE system. Through an **IEEE 1149** .1 interface, the ADCBIST provides control of stimulus generation and results memory for precision measurements of converter characteristics.
Comprehensive BIST Solution for ADCs
ADCBIST complements...

5/3,K/7 (Item 3 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01271560 Supplier Number: 45037494 (USE FORMAT 7 FOR FULLTEXT)
MENTOR GRAPHICS ANNOUNCES VERILOG SUPPORT IN BSDARCHITECT TEST SYNTHESIS TOOL
News Release, pN/A
Oct 3, 1994
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 823

... defects, the company also announced the availability of standalone diagnostic and fault simulation capabilities in the form of the FastScan7M Diagnostics and FlexTestTM FaultSim products.
" **Boundary** scan design starts continue to increase at a rate of about 30 percent a year, forcing both VHDL and Verilog users to look for ways...

...this reason, Mentor
Graphics is providing DFT tools that support both VHDL and Verilog users."

Olen continued, "To help facilitate the accurate detection of manufacturing **defects** and improve device quality and yields, Mentor **Graphics** is also now offering FastScan Diagnostics and FlexTest **FaultS** 'im as standalone products. With these products, manufacturing engineers can quickly diagnose and simulate faults to minimize device failure rates."

BSDArchitect Automatically Generates **IEEE 1149** .1 and Design Core Logic After describing the core logic of the design with either Verilog or 'VHDL, designers can use BSDArchitect to synthesize and verify **IEEE 1149** .1 **boundary scan** at the register transfer level. The tool then automatically generates a test bench for either VHDL or Verilog simulation, and a hierarchical description of the **boundary scan** , with a description of the core logic. As a result, designers can eliminate costly design iterations and easily meet required timing constraints. To help reduce non- recurring engineering (NRE) costs, BSDArchitect offers retargetability capabilities that enable designers to re-use **boundary scan** descriptions in other devices, independent of vendor.

FastScan Diagnostics Increase Manufacturing Process Quality During the device manufacturing process, users of FastScan Diagnostics can detect, isolate, and determine the cause of device failures to improve process yield. FastScan Diagnostics is the EDA industry's only low-cost **fault** diagnosis tool containing proven technology available in Mentor **Graphics** ' industry-leading FastScan ATPG tool. FastScan iagnostics accepts as input, **failing** test pattern data including pattern number and pin or scan cell with a difference. The tool automatically simulates a fault until it finds a difference ...

5/3,K/8 (Item 4 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01260241 Supplier Number: 44752968 (USE FORMAT 7 FOR FULLTEXT)
MOTOROLA STANDARDIZES ON MENTOR GRAPHICS' FASTSCAN TEST TOOLS
News Release, pN/A
June 13, 1994
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 698

... rule-checking, automatic test pattern generation, fast fault simulation, built-in-self-test support, and diagnostics. FastScan also supports stuck-at, 1DDQ toggle, and transition **fault** models. FastScan is a key component of Mentor **Graphics1** top- down Design-Solver Test products portfolio, which also includes FlexTestTM for partial/sequential scan, DFTAdvisor for automatic test insertion, QuickFault II for deterministic fault simulation, QuickGrade II for statistical fault grading, QuickPathTM for critical timing analysis, and the recently introduced BSDArchitect for automatic test synthesis and verification of **boundary scan** logic.

Motorola's OACS system will include FastScan support on Sun SPARC and HP7XX platforms in the third quarter of 1994 for beta sites and...

5/3,K/9 (Item 5 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01253863 Supplier Number: 44619786 (USE FORMAT 7 FOR FULLTEXT)
MENTOR GRAPHICS DEBUTS EDA INDUSTRY'S FIRST AUTOMATED VHDL BOUNDARY SCAN TOOL FOR REDUCED TEST DEVELOPMENT
News Release, pN/A
April 25, 1994

Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 763

... integrated with Mentor Graphics' Design-
Solver Test products, including DFTAdvisorTN for automated scan insertion and testability analysis; FastScanTM, for high test coverage of full-scan, **boundary scan**
and built-in-self-test designs;
FlexTest1M, for non-, partial-, full-scan, and **boundary scan**
designs;
QuickFaultTM II, for fast, accurate timing-based simulation, and QuickGrade1M ((for statistical **fault** grading. BSDArchitect is also integrated with Mentor **Graphics** ' Top Down Design-SolverTM and System Design StationTM products.
Price and Availability
BSDArchitect is priced at $25,000 for a floating license and will be...

...automated design-for-test tools. The company's engineers work with university researchers, including those at Stanford University, to provide technology for test insertion of **IEEE 1149** .1 **boundary scan**
into VHDL digital circuit descriptions. The company is located at 22 Haverhill Rd.,
Windham, N.H. 03087-0128.
Established in 1981, Mentor Graphics Corporation (NASDAQ...

5/3,K/10 **(Item 6 from file: 621)**
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01211965 Supplier Number: 43641252 (USE FORMAT 7 FOR FULLTEXT)
New L321 Combinational Tester Lowers Cost of Testing High- Performance Circuit Boards
News Release, pN/A
Feb 9, 1993
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1038

... L321's substantial size and cost
reductions on new projects.

The L321 allows manufacturers to use a mix of test techniques in-circuit, functional, and **boundary scan** to achieve the highest **fault**
coverage. ProgramGuide (TM), Teradyne's **graphically** guided and structured programming environment, provides a consistent user inteiface for development and debug of all types of tests, helping both new and experienced users...

5/3,K/11 **(Item 7 from file: 621)**
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01188007 Supplier Number: 42843475 (USE FORMAT 7 FOR FULLTEXT)
HP TEST VUE SPEEDS TEST-DEVELOPMENT TIME
News Release, p1
March 20, 1992
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 469

... using data provided by built-in CAD-link software.
Programmers can view the printed-circuit board on their workstation

screen and edit the test data **graphically** . Extensive test analysis allows the programmer to identify potential **problems** early in the test-development process.

Users can generate in-circuit, **boundary - scan** tests for even the most complex parts within minutes using the HP Test VUE tools. The software automatically generates the test for the part based on the **boundary - scan** description language.

Debug Minimized

The tool set automatically manages engineering change orders by scheduling the minimum number of steps needed to implement a given change...

5/3,K/12 (Item 8 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01186098 Supplier Number: 42776674 (USE FORMAT 7 FOR FULLTEXT)
Teradyne debuts new board test systems and software for "reduced-contact test" at NEPCON West
News Release, pN/A
Feb 25, 1992
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 967

... avionics, and weapons systems are verified."

The new RCT products include the L323 test system, which supports edge-to-edge and cluster functional testing and **boundary - scan** testing of VLSI boards and modules with digital, analog, scan, and memory devices. With U.S. list prices starting at $400,000 and data rates...

...ProgramGuide (TM), a graphical programming environment that structures programming processes; ExpressLink (TM), a concurrent engineering tool that generates and verifies functional test programs on Mentor **Graphics** design systems; and ExpertMatch (TM), enhanced **fault** -dictionary diagnostics for Teradyne L300 testers.

"The market has given us the message that they need solutions to the lack of nodal access for test...

5/3,K/13 (Item 9 from file: 621)
DIALOG(R)File 621:Gale Group New Prod.Annou.(R)

01159935 Supplier Number: 41999990 (USE FORMAT 7 FOR FULLTEXT)
UTMC INTRODUCES SYSTEM-LEVEL MEGAFUNCTIONS FOR 1.2-MICRON GATE ARRAY FAMILY
News Release, p1
April 11, 1991
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 664

... reliability and testability are increased by using JTAG-compatible scan cells to meet user-defined Built-In Self-Test (BIST) requirements as well as the **IEEE 1149** .1 standard for serial boundary - **scan** testability.

Up to 256 TTL- or CMOS-compatible signal I/Os are fully programmable

as receiver, driver, or bi-directional, three-state, or open drain...

...Also,
internal clock drivers reduce clock skew, resulting in consistent performance across the array.

UTMC provides software toolkits, with schematic capture and simulation, for Mentor **Graphics** (R) and Valid (TM) workstations. Layout, design verification, **fault** grading, and system-level simulation are also available.

The megafunctions are available on the UTE-R arrays in the following pingrid array and flatpack packaging...

5/3,K/14 (Item 1 from file: 636)
DIALOG(R)File 636:Gale Group Newsletter DB(TM)

01749857 Supplier Number: 42882890 (USE FORMAT 7 FOR FULLTEXT)
Teradyne Introduces Reduced-Contact Test System
SMT Trends, v9, n3, pN/A
April, 1992
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 277

... avionics, and weapons systems are verified."
The new RCT products include the L323 test systems, which support edge-to-edge and cluster functional testing, and **boundary - scan** testing, of both VLSI boards and modules with digital, analog, scan, and memory devices. With US list prices starting at $400,000 and data rates...

...are ProgramGuide, a graphical programming environment that structures the programming process; ExpressLink, a concurrent engineering tool that generates and verifies functional test programs on Mentor **Graphics** design systems; and ExpertMatch, enhanced **fault** -dictionary diagnostics for Teradyne L300 testers.
"The market has given us the message that they need solutions to the lack of nodal access for test...

5/3,K/15 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

04694238 Supplier Number: 46909445 (USE FORMAT 7 FOR FULLTEXT)
UTR 0.8 mu m family is made for space
Electronics Times, p10
Nov 21, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 265

... has a three-level metal technology, and runs with clock speeds of 130MHz at a supply of 5V. On-chip test is provided by ITAG **boundary scan** registers.
The family can withstand a total ionising dose of one million rads, and has single event upset immunity to less than 0.00000000001 **errors** /bit/day.
EDA tool support is provided by Mentor **Graphics** , Synopsys and VHDL tools on Hewlett-Packard and Sun workstations. The cell library has more than 170 options, including ram, MIL-STD-1553, MIL-STD...

5/3,K/16 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

04633582 Supplier Number: 46816541 (USE FORMAT 7 FOR FULLTEXT)
System houses, tool makers tap new techniques to conquer 'uphill battle': Testing bedevils deep-submicron design
Electronic Engineering Times, p47
Oct 21, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 3442

... to ramp up," said Steve Smith, director of marketing at Sunrise, one of the big three in scan-based ATPG testing (the others are Mentor **Graphics** and Synopsys). "New **fault** models then will be embodied in new tools," Smith added.
'Developing new models is but one of many new issues. As the last decade of...

...technology. The vectors generated by this process then go to the ASIC vendor for use in manufacturing test.
Augmenting that flow are BIST and perhaps **boundary - scan** techniques to deal with embedded memories and surrounding logic.
That scenario will die with the century. As density deepens, new requirements will demand a new...

5/3,K/17 **(Item 3 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)

03063799 Supplier Number: 44170339 (USE FORMAT 7 FOR FULLTEXT)
Design-for-test to star at ITC
Electronic Engineering Times, p4
Oct 18, 1993
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1589

... will release its TestBench ATPG tool at ITC. Marketed by IBM's Altium subsidiary (Burbank, Calif.), the TestBench tool is surrounded by design rule checkers, **graphical** interfaces, hypertext help, **fault** simulation and other capabilities designed to ease the burden of adding testability. The tool is targeted at the level-sensitive and edge-sensitive scan methodologies...

...manufacturing faults like shorted nets,' said Brian Keller, the lead architect of TestBench. 'Users or ASIC manufacturers can define those faults.'
But after internal- and **boundary - scan** cells have been inserted, then what? For designers, there has been precious little in the way of prototype debugging tools that take advantage of scan...

5/3,K/18 **(Item 4 from file: 16)**
DIALOG(R)File 16:Gale Group PROMT(R)

02736855 Supplier Number: 43662980 (USE FORMAT 7 FOR FULLTEXT)
HP adds new twist to edge-card test
Electronic Engineering Times, p60
Feb 22, 1993
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 418

... Moore said.
One result of transferring core IC test technology to the functional board-test arena is that users will be able to quickly trace **faults** to the **failing** location using, among other things, a **graphical**

back-tracing technique supported by a **fault** dictionary.

Another key aspect of the 82000FT is software that adapts tools from Mentor **Graphics** for manufacturing test. The tools predict **fault** coverage and model, or simulate, the characteristics of both the tester and test fixture. Also included are facilities for testing mixtures of **boundary - scan** and non- **boundary - scan** devices - important for those building MCM devices.

The base price of the HP machine is $350,000.

Call (303) 679-5000

5/3,K/19 (Item 5 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

02136429 Supplier Number: 42772751 (USE FORMAT 7 FOR FULLTEXT)
Teradyne Offers 'Reduced-Contact' Testers
Electronic News (1991), p22
Feb 24, 1992
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 432

... 400,000 to $600,000; on the 353 from $600,000 to $800,000 and on the 357 from $800,000 to $1 million.

When **boundary scan** components co-exist with non-scannable devices on the same board, fault modeling and test program development can be challenging. Teradyne believes that a "structured...

...OSF/Motif user interface, it depicts each step of the programming process as a flow diagram.

Also new on the software front is ExpertMatch, a **fault** dictionary diagnostic package.

Teradyne has also brought out Mentor **Graphics** ExpressLink, a concurrent engineering tool that generates complete test programs with diagnostics from Mentor design packages.

All the new software packages are to be available...

5/3,K/20 (Item 6 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

02136338 Supplier Number: 42772660 (USE FORMAT 7 FOR FULLTEXT)
Testers work around lack of node access
Electronic Engineering Times, p55
Feb 24, 1992
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 464

... Teradyne's Victory software (as an option). Victory carries a suite of tools to verify internal logic and to track down problems in both the **boundary - scan** and non- **boundary - scan** components, including shorts and opens.

Thus, the edge connector becomes the "point of visibility" for fault coverage, despite limited nodal access. However, such a strategy...

...productivity: ProgramGuide, ExpressLink and ExpertMatch.

Briefly, ProgramGuide is a graphical environment for structured programming; ExpressLink is a concurrent tool for producing test programs on Mentor **Graphics** Corp. design systems; and ExpertMatch provides diagnostics for identifying **failing** devices.

ProgramGuide - based on the Motif and X Window standards - **graphically** guides users through a structured flow-diagram process, controlling program execution. By modeling members of the RCT family, among other things, ExpressLink can validate the...

5/3,K/21 **(Item 1 from file: 148)**
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2004 The Gale Group. All rts. reserv.

09060915 SUPPLIER NUMBER: 18800651 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Testing bedevils deep-submicron design. (system houses and tool makers tappng new techniques)(Special Report: Testing) (Technology Information)
Runyon, Stan
Electronic Engineering Times, n924, p47(3)
Oct 21, 1996
ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 3750 LINE COUNT: 00297

... to ramp up," said Steve Smith, director of marketing at Sunrise, one of the big three in scan-based ATPG testing (the others are Mentor **Graphics** and Synopsys). "New **fault** models then will be embodied in new tools," Smith added.
Developing new models is but one of many new issues. As the last decade of...

...technology. The vectors generated by this process then go to the ASIC vendor for use in manufacturing test.
Augmenting that flow are BIST and perhaps **boundary - scan** techniques to deal with embedded memories and surrounding logic.
That scenario will die with the century. As density deepens, new requirements will demand a new...

5/3,K/22 **(Item 2 from file: 148)**
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2004 The Gale Group. All rts. reserv.

07312647 SUPPLIER NUMBER: 16140920 (USE FORMAT 7 OR 9 FOR FULL TEXT)
'DFT is becoming mandatory.' (design-for-test: electronic engineering process)(includes related article on boundary scanning)
Parry, Simon
Electronics Weekly, n1683, p16(1)
June 1, 1994
ISSN: 0013-5224 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1321 LINE COUNT: 00099

... receive a mixed reception - although the situation is changing. Engineers continue to use partial and full scan test methodologies but are increasingly willing to use **boundary scan** because of its commercial support. This applies both to design tools and to the availability of ICs with JTAG structures.
An Asic designer will not...

...logic core.
There are a variety of tools which warn of test problems, insert scan-paths in logic, automatically generate test vectors and report the **fault** coverage achieved. Mentor **Graphics** , for instance, has DFT Advisor and two automatic test pattern generation (ATPG) tools for full and partial methodologies. The DFT Advisor warns of impending test...

5/3,K/23 **(Item 1 from file: 647)**
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2004 CMP Media, LLC. All rts. reserv.

01107669 CMP ACCESSION NUMBER: EET19961021S0138
System houses, tool makers tap new techniques to conquer 'uphill battle' - Testing bedevils deep-submicron design
Stan Runyon
ELECTRONIC ENGINEERING TIMES, 1996, n 924, PG47
PUBLICATION DATE: 961021
JOURNAL CODE: EET LANGUAGE: English

RECORD TYPE: Fulltext
SECTION HEADING: Design - Special Report
WORD COUNT: 3461

... to ramp up," said Steve Smith, director of marketing at Sunrise, one of the big three in scan-based ATPG testing (the others are Mentor **Graphics** and Synopsys). "New **fault** models then will be embodied in new tools," Smith added.

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...technology. The vectors generated by this process then go to the ASIC vendor for use in manufacturing test.

Augmenting that flow are BIST and perhaps **boundary - scan** techniques to deal with embedded memories and surrounding logic.

That scenario will die with the century. As density deepens, new requirements will demand a new...

5/3,K/24 (Item 2 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

00535080 CMP ACCESSION NUMBER: EET19930222S5370
HP adds new twist to edge-card test
STAN RUNYON
ELECTRONIC ENGINEERING TIMES, 1993, n 734, 60
PUBLICATION DATE: 930222
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Design - Test & Measurement
WORD COUNT: 425

... Moore said.

One result of transferring core IC test technology to the functional board-test arena is that users will be able to quickly trace **faults** to the **failing** location using, among other things, a **graphical** back-tracing technique supported by a **fault** dictionary.

Another key aspect of the 82000FT is software that adapts tools from Mentor **Graphics** for manufacturing test. The tools predict **fault** coverage and model, or simulate, the characteristics of both the tester and test fixture. Also included are facilities for testing mixtures of **boundary - scan** and non- **boundary - scan** devices-important for those building MCM devices.

The base price of the HP machine is $350,000.

Call (303) 679-5000

Reader Service No. 154

5/3,K/25 (Item 3 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext

00530870 CMP ACCESSION NUMBER: EET19931018S1156
Design-for-test to star at ITC
STAN RUNYON
ELECTRONIC ENGINEERING TIMES, 1993, n 768, 4
PUBLICATION DATE: 931018
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: News
WORD COUNT: 1607

... will release its TestBench ATPG tool at ITC. Marketed by IBM's Altium subsidiary (Burbank, Calif.), the TestBench tool is surrounded by design rule checkers, **graphical** interfaces, hypertext help, **fault** simulation and other capabilities designed to ease the burden of adding testability. The tool is targeted at the level-sensitive and

edge-sensitive scan methodologies...

...manufacturing faults like shorted nets," said Brian Keller, the lead architect of TestBench. "Users or ASIC manufacturers can define those faults."

But after internal- and **boundary - scan** cells have been inserted, then what? For designers, there has been precious little in the way of prototype debugging tools that take advantage of scan...

5/3,K/26 (Item 1 from file: 810)
DIALOG(R)File 810:Business Wire
(c) 1999 Business Wire . All rts. reserv.

0467629 BW1250

GENRAD 2: Genrad improves productivity of its high-efficiency GR228X family of Board Test Systems with release 3.01

March 01, 1995

Byline: Business Editors

...we focused on user utility for those seeking enhanced analog test tools and increased productivity. Release 3.01 is exceptionally 'new-feature-rich,' including a **graphical** program- optimization toolset - Analog **Graphical** Debug Station, Analog **Fault** Coverage Report, Analog Component Library Toolset, and a new **boundary - scan** test generator for our Scan Pathfinder Graphical User Interface. These are in addition to the recently introduced Release 2.1 features such as Data Display...

5/3,K/27 (Item 1 from file: 610)
DIALOG(R)File 610:Business Wire
(c) 2004 Business Wire. All rts. reserv.

00826217 20021218352B7466 (USE FORMAT 7 FOR FULLTEXT)
Goyatek Technology Standardized on Mentor Graphics Design-for-Test Tools
Business Wire
Wednesday, December 18, 2002 09:02 EST
JOURNAL CODE: BW LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
DOCUMENT TYPE: NEWSWIRE
WORD COUNT: 760

...application times, facilitates high test set reusability and produces the high quality test. The BSDArchitect tool dramatically reduces development time by automating the implementation of **boundary scan** circuitry. The tool's flexible test access port (TAP) synthesis engine supports any **boundary scan** configuration to thoroughly test internal structures such as memory BIST, embedded cores and IP.

"As our customers face more complex design challenges we need to be ready with advanced test solutions that can be used now," said Robert Hum, vice president and general manager, Design Verification and Test group, Mentor **Graphics** . "The move to nanometer processes introduce **problems** that are difficult to detect and can have a tremendous impact on yield. By enhancing capabilities such as at-speed test we are able to...

...DFT solutions

for today's System-on-Chip and deep submicron designs and includes solutions
for ATPG, embedded deterministic test, memory BIST, logic BIST, and **boundary**
scan . Mentor Graphics DFT Centers of Excellence are located worldwide and employ the industry's leading professionals in the research and application of
proven DFT solutions...

5/3,K/28 **(Item 1 from file: 813)**
DIALOG(R)File 813:PR Newswire

1359426 HSM042
Mentor Graphics Announces Industry's Only BIST Software For Testing at True Operating Speeds;

DATE: October 19, 1998 09:36 EDT WORD COUNT: 1,836

... design. The CTIntegrator tool simplifies the testing of complex core-based designs by integrating various DFT methodologies, such as BIST, full scan, partial scan, and **boundary scan** . The tool also provides an access mechanism to test cores that are delivered with pre-computed test vectors -- a typical scenario for legacy cores. By...

... structures and DFT methodologies of multiple cores, the CTIntegrator tool creates a comprehensive SOC test environment that takes complete advantage of existing test patterns and **fault** coverage.

CONTACT: Michelle Clancy, Marketing Communications, of Mentor **Graphics** Corporation, 503-685-4830, or michelle clancy mentorg.com; or Lisa Wood, Public Relations of KVO, 503-221-2361, or lisa wood kvo.com, for ...

5/3,K/29 **(Item 2 from file: 813)**
DIALOG(R)File 813:PR Newswire

1292230 SFM026
Mentor Graphics' Design-for-Test and Static Timing Analysis Tools Jump-Start ASIC Council's Open Library API (OLA) Standard

DATE: June 15, 1998 09:30 EDT WORD COUNT: 869

... TM) for memory BIST synthesis; LBISTArchitect(TM) for logic BIST synthesis; DFTAdvisor and DFTInsight(TM) for testability analysis and scan test synthesis; BSDArchitect(TM) for **IEEE 1149** .1 **boundary scan** synthesis; FastScan for full-scan and structured partial-scan ATPG; and FlexTest(TM) for partial-scan and non-scan ATPG.

SST Velocity

SST Velocity from...

... including asynchronous clocks; and industry-leading ease-of-use features. These features give the designer the ability to quickly find, and fix, the sources of **problems** .

Mentor **Graphics** Corporation is a world leader in electronic hardware and software design solutions, providing products and consulting services for the world's largest electronics and semiconductor...

File 347:JAPIO Nov 1976-2004/Feb(Updated 040607)
(c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200442
(c) 2004 Thomson Derwent

Set	Items	Description
S1	840	BOUNDARY()SCAN OR (IEEE OR ENGINEER???)(2W)1149
S2	75611	GRAPHIC? OR GUI? ?
S3	1877	S2(10N)(FAULT? ? OR FAIL??? OR VIOLAT? OR ERROR? ? OR DEFECT? OR PROBLEM? OR FLAW? ? OR IRREGULAR? OR INVALID? OR ("NOT" OR T)(1W)(VALID OR ACCURAT?) OR INACCURAT? OR ABNORMAL?)
S4	2	S1 AND S3

4/5/1 **(Item 1 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

016272322 **Image available**
WPI Acc No: 2004-430216/200440
XRPX Acc No: N04-340116
Apparatus for isolating faulty **semiconductor device in multiple format video** graphic **system, isolates** fault **device such as buffer, convolver and router based on contents of signature register and format of data frame**
Patent Assignee: CHEUNG T C (CHEU-I)
Inventor: CHEUNG T C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040088638	A1	20040506	US 2002267809	A	20021009	200440	B

Priority Applications (No Type Date): US 2002267809 A 20021009
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040088638	A1		14	H03M-013/00	

Abstract (Basic): US 20040088638 A1
NOVELTY - A buffer (107) receives data frame in any one of multiple formats. A convolver (120) including a signature register receives frame from the buffer, and determines the format of the frame. An analyzer (140) isolates the fault semiconductor device such as buffer, convolver and a router (130), and the faulty interconnect based on the contents of the signature register and determined format.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(1) method for isolating faulty semiconductor device; and
(2) multiple format video graphic system.
USE - For isolating **faulty** semiconductor device in multiple format video **graphic** system (claimed).
ADVANTAGE - Enables to detect and isolate more than one **faulty** device in the multiple format video **graphic** system.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the multiple format video graphic system.
video source (105)
buffer (107)
convolver (120)
video output device (125)
router (130)
analyzer (140)
pp; 14 DwgNo 1/5
Title Terms: APPARATUS; ISOLATE; FAULT; SEMICONDUCTOR; DEVICE; MULTIPLE; FORMAT; VIDEO; GRAPHIC; SYSTEM; ISOLATE; FAULT; DEVICE; BUFFER; CONVOLVER ; ROUTER; BASED; CONTENT; SIGNATURE; REGISTER; FORMAT; DATA; FRAME
Derwent Class: T01; U11
International Patent Class (Main): H03M-013/00
File Segment: EPI

4/5/2 **(Item 2 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

016216148 **Image available**
WPI Acc No: 2004-374036/200435
XRPX Acc No: N04-297525
Faulty **semiconductor device isolating apparatus for video** graphics **system, has signature analyzer that isolates** faulty **semiconductor device and** faulty **interconnection using multiple bits stored in signature register in convolver**
Patent Assignee: CHEUNG T C (CHEU-I)
Inventor: CHEUNG T C

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040073858	A1	20040415	US 2002267804	A	20021009	200435	B

Priority Applications (No Type Date): US 2002267804 A 20021009
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040073858	A1		13	G01R-031/28	

Abstract (Basic): US 20040073858 A1

NOVELTY - A signature analyzer (140) isolates the faulty semiconductor device and the faulty interconnection by using multiple bits stored in the signature register in a convolver (120).

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) method for isolating faulty semiconductor devices; and

(2) system for isolating faulty semiconductor device.

USE - For isolating **faulty** semiconductor devices in modern video **graphics** system such as Sun Micro system, video graphic system for providing video data to variety of output devices including video projectors, television, monitor, etc.

ADVANTAGE - Enables easy operation.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the faulty semiconductor device isolating apparatus.

video graphics system (110)

convolver (120)

video output device (125)

router (130)

signature analyzer (140)

pp; 13 DwgNo 1/5

Title Terms: FAULT; SEMICONDUCTOR; DEVICE; ISOLATE; APPARATUS; VIDEO; GRAPHIC; SYSTEM; SIGNATURE; ANALYSE; ISOLATE; FAULT; SEMICONDUCTOR; DEVICE; FAULT; INTERCONNECT; MULTIPLE; BIT; STORAGE; SIGNATURE; REGISTER; CONVOLVER

Derwent Class: S01; T01

International Patent Class (Main): G01R-031/28

File Segment: EPI

File 348:EUROPEAN PATENTS 1978-2004/Jun W03
(c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20040701,UT=20040624
(c) 2004 WIPO/Univentio

Set	Items	Description
S1	804	BOUNDARY()SCAN OR (IEEE OR ENGINEER???)(2W)1149
S2	125439	GRAPHIC? OR GUI? ?
S3	4631	S2(10N)(FAULT? ? OR FAIL??? OR VIOLAT? OR ERROR? ? OR DEFECT? OR PROBLEM? OR FLAW? ? OR IRREGULAR? OR INVALID? OR ("NOT" OR T)(1W)(VALID OR ACCURAT?) OR INACCURAT? OR ABNORMAL?)
S4	1	S1(100N)S3

4/3,K/1 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00937410 **Image available**

METHOD AND APPARATUS FOR DIAGNOSING FAILURES IN AN INTEGRATED CIRCUIT USING DESIGN-FOR-DEBUG (DFD) TECHNIQUES

PROCEDE ET APPAREIL PERMETTANT DE DIAGNOSTIQUER DES PANNES DANS UN CIRCUIT INTEGRE A L'AIDE DE TECHNIQUES DE DEPANNAGE INTEGREES

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Patent and Priority Information (Country, Number, Date):
Patent: WO 200271567 A1 20020912 (WO 0271567)
Application: WO 2002US3413 20020228 (PCT/WO US0203413)
Priority Application: US 2001272064 20010301; US 200286214 20020227

Designated States: AU BR CA CN CZ ID IL IN JP KP KR MX NO NZ PL RO SG US VN ZA
(EP) AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
(EA) AM AZ BY KG KZ MD RU TJ TM

Publication Language: English
Filing Language: English
Fulltext Word Count: 19213

Fulltext Availability:
Claims

Claim

... controller in said integrated circuit further comprises means for connecting said TAP controller on said low-cost DFT debugger to said integrated circuit through other **boundary - scan** controlled integrated circuits on said evaluation board or system,

7 9 . The apparatus of claim 76,, wherein said **fault** diagnosis program and wherein said **graphical** user interface are selectively performed remotely through internet,